AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 1, 4, 13, 19, and 42, and add new claims 43-48, as shown below .

The following is a complete list of all claims in this application.

1. (Currently Amended) A method for manufacturing a contact structure, comprising steps of:

forming a first conductive layer formed of an aluminum or aluminum alloy ~~aluminum-based~~ material;

depositing an insulating layer; ~~a silicon nitride layer at a temperature between about 280° C and about 400° C;~~

forming a contact hole extending through the insulating ~~silicon nitride~~ layer and exposing the aluminum or aluminum alloy material of the first conductive layer; and

forming a second conductive layer formed of indium zinc oxide (IZO) and directly contacting the aluminum or aluminum alloy material of the first conductive layer through the contact hole.

2-3. (Cancelled)

4. (Currently Amended) The method of claim 1, wherein the step of depositing the ~~silicon nitride~~ insulating layer is performed for about 5 minutes to about 40 minutes.

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5. (Previously Presented) The method of claim 1, wherein the contact hole has a size between about 0.5 mm X 15 μm and 2 mm X 60 μm.

6. (Previously Amended) The method of claim 1, wherein a contact resistance between the first conductive layer and the second conductive layer is less than 10% of a resistance of the first conductive layer.

7. (Original) The method of claim 6, wherein the contact resistance is less than 0.15 $\mu\Omega cm^2$.

8-12. (Cancelled)

13. (Currently Amended) A method for manufacturing a thin film transistor (TFT) array panel, comprising steps of:

depositing a first conductive layer formed of aluminum or aluminum alloy ~~an aluminum-based~~ material on a substrate;

patterning the first conductive layer to form a gate line and a gate pad connected to the gate line;

depositing an insulating ~~a silicon nitride~~ layer on the gate line and [[a]] the gate pad ~~at a temperature between about 280° C and about 400° C~~;

forming a semiconductor layer on the insulating ~~silicon nitride~~ layer;

depositing a second conductive layer on the semiconductor layer;

patterning the second conductive layer to form a data line;

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forming a contact hole extending through insulating the ~~silicon nitride~~ layer and exposing the aluminum or aluminum alloy material of the gate pad;

depositing a third conductive layer formed of an indium zinc oxide (IZO) layer; and

patterning the third conductive layer to form a conductive pattern directly contacting the aluminum or aluminum alloy material of the gate pad in the contact hole.

14-15. (Cancelled)

16. (Previously Amended) The method of claim 13, wherein the step of depositing the third conductive layer comprises a step of sputtering a compound including In_2O_3 and ZnO.

17. (Previously Presented) The method of claim 16, wherein a content rate of Zn in the compound is between about 15% and about 20%.

18. (Previously Amended) The method of claim 13, wherein the step of patterning the third conductive layer comprises a step of forming a pixel electrode connected to the data line.

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19. (Currently Amended) A method for manufacturing a thin film transistor array panel, comprising steps of:

depositing a first conductive layer formed of aluminum or aluminum alloy ~~an aluminum-based~~ material on a substrate;

patterning the first conductive layer to form a gate line, a gate electrode and a gate pad;

depositing a gate insulating layer ~~a silicon nitride layer at a temperature between about 280° C and about 400° C~~;

forming a semiconductor layer on the gate insulating ~~silicon nitride~~ layer;

depositing a second conductive layer over the silicon nitride layer and the semiconductor layer;

patterning the second conductive layer to form a data line, a source electrode and a drain electrode;

forming a passivation layer over the silicon nitride layer and the data ~~wire~~ line;

forming a contact hole extending through the passivation layer and the gate insulating ~~silicon nitride~~ layer and exposing the aluminum or aluminum alloy material of the gate pad;

depositing a third conductive layer formed of an indium zinc oxide (IZO) layer over the passivation layer; and

patterning the third conductive layer to form a redundant gate pad directly contacting the aluminum or aluminum alloy material of the gate pad through the contact hole.

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20. (Previously Amended) The method of claim 19, wherein the step of patterning the third conductive layer comprises a step of patterning the third conductive layer to form a pixel electrode.

21. (Previously Amended) The method of claim 19, wherein the step of patterning the second conductive layer comprises a step of patterning the second conductive layer to form a data pad, and

the step of patterning the third conductive layer comprises a step of patterning the third conductive layer to form a redundant data pad connected to the data pad.

22. (Previously Presented) The method of claim 19, wherein the step of forming the passivation layer comprises a step of depositing a silicon nitride layer at a temperature between about 280° C and about 400° C.

23. (Cancelled)

24. (Previously Amended) The method of claim 19, wherein the step of depositing the third conductive layer comprises a step of sputtering a compound including In_2O_3 and ZnO.

25. (Previously Presented) The method of claim 24, wherein a content rate of Zn in the compound is between about 15% and about 20%.

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26. (Previously Amended) The method of claim 19, wherein the step of patterning the second conductive layer comprises a step of patterning the semiconductor layer and the second conductive layer simultaneously by using a photoresist pattern having portions with different thicknesses.

27. (Previously Presented) The method of claim 26, wherein the photoresist pattern comprises a first portion having a first thickness, a second portion having a second thickness greater than the first thickness, and a third portion having a third thickness smaller than the first thickness.

28. (Previously Presented) The method of claim 27, wherein a mask used for forming the photoresist pattern has a first area having a first transmittance, a second area having a second transmittance smaller than the first transmittance, and a third area having a third transmittance greater than the first transmittance.

29. (Previously Amended) The method of claim 28, wherein the first portion of the photo resist pattern is aligned on a portion between the source electrode and the drain electrode, and the second portion of the photoresist pattern is aligned on the data line.

30. (Previously Presented) The method of claim 29, wherein the first area of the mask includes a partially transparent layer or a pattern reducing a transmittance.

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31. (Previously Presented) The method of claim 30, wherein the first thickness is less than a half of the second thickness.

32. (Previously Amended) The method of claim 31, further comprising a step of depositing an ohmic contact layer between the source and drain electrodes and the semiconductor layer.

33. (Previously Amended) The method of claim 32, wherein the second conductive layer, the ohmic contact layer, and the semiconductor layer are patterned by a single photolithography process.

34-41. (Cancelled)

42. (Currently Amended) A method for manufacturing a contact structure, comprising steps of:

depositing a first conductive layer formed of aluminum on a substrate;

patterning the first conductive layer to form a signal line;

depositing a silicon nitride layer on the signal line at a fixed temperature between about 280° C and about 400° C;

forming a contact hole extending through the silicon nitride layer and exposing the aluminum signal line; and

forming a second conductive layer formed of indium zinc oxide (IZO) and directly contacting the aluminum signal line through the contact hole.

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43. (New) The method for manufacturing contact structure according to the claim 1, further comprising, preheating the first conductive layer before forming the second conductive layer.

44. (New) The method for manufacturing a thin film transistor (TFT) array panel according to the claim 13, further comprising, preheating the passivation layer, the silicon nitride layer and the exposed gate pad before the forming the third conductive layer.

45. (New) The method of claim 1, wherein the first insulating layer is comprised of silicon nitride.

46. (New) The method of claim 45, wherein the first insulating layer of silicon nitride is deposited at a temperature between about 280° C and about 400° C.

47. (New) The method of claim 13, wherein the insulating layer is comprised of silicon nitride.

48. (New) The method of claim 47, wherein the insulating layer of silicon nitride is deposited at a temperature between about 280° C and about 400° C.

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